AF/2815 *IFW* 

#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: DAVIES, ROBERT B.

Serial No.: 09/920,222

Ex: LEE

Filed:

01 AUGUST 2001

Art Unit: 2815

For:

SEMICONDUCTOR DEVICE WITH INDUCTIVE COMPONENT AND

METHOD OF MAKING

## CERTIFICATE OF MAILING

Commissioner Of Patents P.O. Box 1450 Alexandria, VA 22313-1450 Mail Stop Appeal Brief - Patents

#### Dear Sir:

I hereby certify that the attached Transmittal of Appeal Brief; Supplemental Appeal Brief for Appellants and two (2) copies of same; and a postcard are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents P.O. Box 1450, Alexandria, VA 22313-1450, Mail Stop Non-Fee Amendment on 18 May 2004.

Mandy Velasculz Signature Velasculz

18 May 2004

Date 5/18/04

Respectfully Submitted,

Robert A. Parsons Attorney for Applicant

Reg. No. 32,713

340 East Palm Lane Suite 260 Phoenix, Arizona 85004 (602) 252-7494



#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: DAVIES, ROBERT B.

Serial No.: 09/920,222 ) Ex: LEE

Filed: 01 AUGUST 2001 ) Art Unit: 2815

For: SEMICONDUCTOR DEVICE WITH)

INDUCTIVE COMPONENT AND )
METHOD OF MAKING

TRANSMITTAL OF SUPPLEMENTAL APPEAL BRIEF

Mail Stop Appeal Brief-Patents Commissioner For Patents P.O. Box 1450 Alexandria VA 22313-1450

Dear Sir:

Enclosed is the Supplemental Appeal Brief For Appellants and two copies of the same, in compliance with the Rules, in the above captioned matter; and a postcard.

Respectfully submitted,

Robert A. Parsons

Attorney for Applicant Registration No. 32,713

18 May 2004

340 East Palm Lane Suite 260 Phoenix, Arizona 85004

(602) 252-7494



#### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Date:

11 May 2004

Robert B. Davies

Art Unit: 2815

Serial No.: 09/920,222

Filed: 01 August 2001

Examiner: Lee, Eugene

For:

SEMICONDUCTOR DEVICE WITH

INDUCTIVE COMPONENT AND

METHOD OF MAKING

# SUPPLEMENTAL APPEAL BRIEF FOR APPELLANT

MAIL STOP APPEAL BRIEF Commissioner for Patents P.O. Box 1450 Alexandria VA 22313-1450

SIR:

In response to Appellant's Appeal Brief mailed on 18 December 2003, the Examiner in this case reopened prosecution and submitted a non-final Office Action (hereinafter "the ACTION"), which was mailed on 7 April 2004. Rather than file a specific reply to the ACTION under 37 C.F.R. § 1.111, appellant hereby responds to the ACTION by requesting reinstatement of the appeal and consideration of this Supplemental Appeal Brief, as well as the Brief.

# I. NEW ISSUES FOR REVIEW IN THE 11 February 2003 NON-FINAL OFFICE ACTION

The new issues for review are:

- 1.) Whether the drawings show every feature of the claimed invention?
- 2.) Whether the language, "the pedestal" in claim 47 is indefinite for lack of antecedent basis?
- 3.) Whether claims 1-3, 5-7, 37-40, 42, 43, 45, and 47-50 are unobvious and, therefore, patentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000)?
- 4.) Whether claims 4, 41, and 51 are unobvious and, therefore, patentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000), as applied in issue 3 above, and further in view of Matsuzaki (JP. 06-120036)?
- 5.) Whether claims 28-33 are unobvious and, therefore, patentable over Matsuzaki (JP. 06-120036) in view of Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000)?
- 6.) Whether claims 44 and 46 are unobvious and, therefore, patentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000), as applied in issue 3 above, and further in view of Farooq et al. (U.S.P. 6,574,859)?

7.) While no citation of claims or specific language was included, there is at least a suggestion of an issue as to whether appellant has product-by-process limitations in any of his claims.

#### VIII. SUPPLEMENTAL ARGUMENT

# ISSUE #1

In the ACTION, the Examiner objects to the drawings as not showing the sealed cavity claimed in claims 43 and 45. Actually, a "sealed cavity" is claimed in claims 44 and 45-48, with claim 43 only claiming "a cavity". However, one has only to look at FIG. 10 to see that appellant has indeed illustrated the claimed sealed cavity. Referring appellant's specification, page 21, lines 11-13, it is clear that a cavity 76 is formed between the lower surface of conductor 47 (i.e. inductors 50 and 250) and the upper surface 77 of pedestal 74. Clearly this cavity is sealed but if simply placing the components as illustrated should, somehow, be interpreted as not sealing then simply referring to page 22, lines 1-8 should alleviate any doubt. Thus, it is clear the drawings show the claimed sealed cavity and this objection is overcome.

## ISSUE #2

In the ACTION, the Examiner rejects claim 47 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Appellant respectfully traverses this rejection.

The Examiner alleges there is no antecedent basis for the term "the pedestal" in claim 47. Appellant disagrees. In an

Amendment and Response to Final Rejection, mailed 24 September 2003, the only amendment appellant made to the claims was to change claim 47 so that it depended from claim 46, rather than claim 45. This amendment was made in response to a rejection identical to this rejection, which was included in the Final Rejection. In an Advisory Action, mailed 15 October 2003, the Examiner marked the box designated 7 and also marked the box indicating that the amendment would be entered. Claim 47 depends from claim 46, which specifies "a pedestal formed on a surface thereof". Thus, claim 47 is not indefinite and this rejection is overcome.

# ISSUE #3

In the ACTION, the Examiner rejects claims 1 thru 3, 5 thru 7, 37 thru 40, 42, 43, 45, and 47 thru 50, under 35 U.S.C. 103(a), as being unpatentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000). Appellant respectfully traverses this rejection.

It should be noted at the outset that the Examiner has not changed his argument, he has simply cited Riseman as support for the argument that Kendall's isolation region 25 could be air instead of dielectric material. Therefore, all of appellant's previous arguments (see appellant's Brief) still apply and, if not repeated herein, are specifically included by reference.

The Examiner, using Kendall's Fig. 15, has labeled the entire right-hand third of Kendall's structure as the "dielectric region". Further, he is apparently using the structure of Fig. 12 to support his argument. For purposes of this response only and making no admissions, the Examiner must be suggesting that the entire etched area of substrate 2 (shown in Figs. 10 and 11) is the dielectric region. Per his hand-written legend on the drawing included in the ACTION, it appears he is stating that the trench is defined between semiconductor studs 9 in Fig. 12. Per another hand-written legend on the drawing included in the ACTION, the Examiner has labeled the oxide layer 7 on the sides of studs 9 as the "dielectric sidewalls". The Examiner then alleges that the body of metallic core material 12 covered by isolation coating 14 is an inductance.

In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. Stratoflex, Inc. v Aeroquip Corp., 713 F.2d 1530, 218 USPQ 871 (Fed. Cir. 1983); Schenck v Nortron Corp., 713 F.2d 782, 218 USPQ 698 (Fed. Cir. 1983). Further, a prior art reference must be considered in its entirety, i.e. as a whole, including portions that would lead away from the claimed invention. W. L. Gore & Associates, Inc. v Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert.

denied, 469 U.S. 851 (1984). "All words in a claim must be considered in judging patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 165 USPQ 494. 496 (CCPA 1970).

Referring to claim 1 as a prime example of appellant's claim language, if the claim is read in its entirety, as it must be, Kendall's structure and disclosure are substantially different. First, claim 1 calls for "a low resistivity semiconductor substrate having a dielectric region formed therein". Claim 1 then specifies "a trench defined in the dielectric region and including dielectric sidewalls". Claim 1 also states that the trench has dielectric sidewalls. Further, claim 1 specifies that an electroplated conductive material is disposed in the trench to produce an inductance having sides and a bottom, "the sides being bounded by the dielectric sidewalls and the cavity being adjacent the bottom." Taking these limitations as a whole (Stratoflex, Inc.), it is clear that nothing in the structure of Kendall even remotely suggests the claimed structure.

First, dielectric layer 7 on the sidewalls of studs 9 in Kendall are not and cannot be sidewalls of the trench, they are sidewalls 9' of the studs (Kendall specification, column 3, line 61). Second, claim 1 specifies that the inductance has sides "bounded by the dielectric sidewalls". Clearly,

even core 12 of Kendall's inductance is not bounded by the sidewalls 9' of studs 9. In fact, a close look at Fig. 15 clearly shows that a substantial amount of circumfusing oxide material is introduced by Kendall after core 12 is positioned between studs 9.

Digressing for a moment, the Examiner argues on page 9 of the ACTION, that the "applicant's claims only state an INDUCTANCE which is a property, not an entire device". Appellant must respectfully disagree. Words of a claim always have a normal meaning unless otherwise defined by the Referring specification. Webster's to New Universal Unabridged Dictionary, copyrighted 1989, the second listed definition of the word "inductance" is "a piece of equipment providing inductance in a circuit or other system; inductor". Clearly, the words inductance and inductor interchangeable. Further, referring to claim 1 the inductance formed by the electroplated conductive material has sides and When the word "inductance" is used to denote a a bottom. property it does not have sides and a bottom. appellant's claimed inductance is an entire device and not a property.

It is interesting to note that the Examiner supports his argument that Kendall's core 12 is an inductance by pointing to a small portion of Kendall's specification, column 8, lines 66-67. The Examiner's conclusion is taken out of

context. If the entire portion of Kendall's discussion is reviewed (column 8, line 63 through column 9, line 3), one instantly recognizes that Kendall is discussing the inductance of the helical coil with a high permeability core and without a core (Fig.14). This discussion has nothing to do with whether or not the high permeability core has an inductance. The only inductance disclosed by Kendall, which could properly be cited by the Examiner is in the Kendall specification at column 1, lines 35-38. Here Kendal states "in accordance with the present invention, a solid state <u>inductance</u> is formed in a semiconductor slice by providing a conductor circumscribing an insulated core material in a helix configuration." (Accent added.)

Returning to the discussion of claim 1 and Kendall, the third point is that claim 1 calls for a cavity adjacent the bottom of the conductance. Even if, arguendo, Kendall's isolation regions 25, comprising layers 25' and regions 25", are replaced with the air isolation cavities 12 of Riseman, they would not be adjacent the bottom of the inductance. They would not even be adjacent the side of the inductance, since the helix formed by studs 9, the circumfusing oxide material, and a portion of substrate 2 lie between core 12 and isolation region 25. It must be noted here that the Examiner has interpreted core 12 as the inductance and he cannot determine that the helix (studs 9) is the inductance for one portion of

the claim and core 12 is the inductance for another portion of the claim. Appellant can positively state that there is no possible interpretation of the structure of Kendall that could result in a structure similar to appellant's claimed structure.

Interpreting the Kendall disclosure as one of ordinary skill in the art would interpret it, the complete inductance must include the helix formed by selectively interconnecting the upper and lower ends of studs 9 as well as core 12. With this interpretation in mind, it is clear that nothing in Kendall is even remotely similar to appellant's novel structure. Kendall does not teach or otherwise disclose all of the claim limitations and nothing in the teachings of Kendall or Riseman in any way suggest appellant's invention to one of ordinary skill in the art.

The Examiner's statement regarding claims 37, 38, 42, 43, 45, and 49 in which he states "multiple cavities are formed that include oxide layer 7 and layers 25'" is simply not understood. Claim 38 specifies "a trench formed in the dielectric region and including side-walls defined by low dielectric constant material". Claim 37 specifies "the low dielectric constant material includes dielectric material defining an array of cavities therein". Kendall discloses one isolation region 25 between the regions designated active region and dielectric region by the Examiner. Even if,

arguendo, the isolation region of Kendall is replaced with a cavity of Riseman, no array of cavities is formed anywhere in Kendall's structure. Thus, Kendall does not disclose structure similar to the claimed structure.

The Examiner's statement regarding claims 39, 40, 47, 48, and 50 in which he states "the applicant must show that the chosen dimensions are critical" is believed to be mis-applied. Appellant disagrees on two grounds. First, it is well known in the art and explained at some length in appellant's specification (note, for example, pages 5-6, the discussion of the advantages of low permittivity, low dielectric constant, etc.) that any reduction the dielectric constant provides many advantages. A reduction of the effective dielectric constant of the dielectric region by at least ten percent is a substantial reduction. nothing in either Kendall or Riseman suggest anything like appellant's claimed structure. Simply placing numbers in a claim to provide specificity, does not make the claim invalid or obvious. Neither In re Woodruff nor In re Boesch apply in the present situation.

In view of the above, appellant believes that claims 1 thru 3, 5 thru 7, 37 thru 40, 42, 43, 45, and 47 thru 50 are not obvious in view of either Kendall or Riseman individually or in any proper combination and are, therefore, allowable.

# ISSUE #4

In the ACTION, the Examiner rejects claims 4, 41, and 51, under 35 U.S.C. 103(a), as being unpatentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000) as applied above, and further in view of Matsuzaki (JP. 06-120036). Appellant respectfully traverses this rejection.

For all of the reasons stated above, neither Kendall nor Riseman individually or in any proper combination disclose anything even remotely similar to appellant's novel claimed structure. Matsuzaki is cited because he discloses a copper coil. Using the copper suggested by Matsuzaki for core 12 of Kendall does not overcome the deficiencies in the disclosure of Kendall. Further, the helical coil or inductance disclosed by Kendall cannot be made of copper since there is no way to implement it from Kendall's disclosure.

In view of the above, appellant believes that claims 4, 41, and 51 are not obvious in view of either Kendall, Riseman, or Matsuzaki individually or in any proper combination and are, therefore, allowable.

# ISSUE #5

In the ACTION, the Examiner rejects claims 28 thru 33, under 35 U.S.C. 103(a), as being unpatentable over Matsuzaki (JP. 06-120036) in view of Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000). Appellant respectfully traverses this rejection.

28, for example, specifies "a low resistivity semiconductor substrate having a dielectric region formed therein with a cavity adjacent the dielectric region" and "a first inductor of electroplated conductive material formed within a trench defined by the dielectric region, a bottom of the inductor being positioned adjacent the cavity". Nothing in the disclosure of Matsuzaki (or Kendall or Riseman, for that matter) suggests a dielectric region formed in semiconductor substrate, a trench defined by the dielectric region with a first inductor formed therein, and a bottom of the inductor positioned adjacent the cavity. Placing one of Kendall's isolation regions between the transistor and coil in FIG. 2 of Matsuzaki and replacing Kendall's isolation region with one of Riseman's cavities still will not result in a structure similar to that claimed in claim 28. The bottom of the inductor will not be positioned adjacent the cavity. side of the inductor will be closest to the cavity but not necessarily adjacent. Unless one uses appellant's teaching in hindsight, there is no teaching in any of the cited disclosures of the advantages that will result from arrangement similar to appellant's.

In view of the above, appellant believes that claims 28 thru 33 are not obvious in view of either Matsuzaki, Kendall,

or Riseman individually or in any proper combination and are, therefore, allowable.

## ISSUE #6

In the ACTION, the Examiner rejects claims 44 and 46, under 35 U.S.C. 103(a), as being unpatentable over Kendall (U.S.P. 3,881,244) in view of Riseman (4,169,000) as applied above, and further in view of Farooq et al. (U.S.P. 6,574,859). Appellant respectfully traverses this rejection.

Farooq et al. is included for the circuit card 10 on which module substrate 4 is mounted. However, the language of claims 44 and 46 clearly show that the present invention is not even similar to the mounting structure of Farooq et al. As explained in detail above nothing in the teachings or disclosures of Kendall and/or Riseman even vaguely suggest appellant's novel structure. Further, nothing in the teachings or disclosure of Farooq et al. overcome the deficiencies.

Each of claims 44 and 46 specify "a die attach pad with a pedestal formed on a surface thereof" and "the substrate being mounted on the die attach pad with the pedestal positioned in the cavity so as to seal the cavity." Nothing in Farooq et al. even vaguely suggests a pedestal. Further, nothing in Kendall suggests a cavity beneath the inductance which is in a

position to be sealed by the pedestal. The isolation cavities of Riseman are already sealed so that if they are substituted for the isolation regions of Kendal no additional sealing would occur, could occur, or should occur by mounting Kendal on the die attach pad of Farooq et al. Thus, this rejection of claims 44 and 46 has been overcome and these claims are allowable.

# ISSUE #7

While no citation of claims or specific language was included in the portion of the ACTION entitled "Product-by-Process Limitations", there is at least a suggestion of an issue as to whether appellant has product-by-process limitations in any of his claims. Appellant respectfully asserts that no such limitations are present.

In the previous rejections, the Examiner has classified appellant's claimed limitation, "electroplated conductive material", as a process limitation that does not add any structural limitations. Appellant respectfully disagrees.

Claim 1 specifies "electroplated conductive material disposed within the trench to produce an inductance having sides and a bottom". As explained above, the term "inductance" denotes a specific device, especially since it has sides and a bottom. The only inductance disclosed by

Kendall "a solid state <u>inductance</u> is formed in a semiconductor slice by providing a conductor circumscribing an insulated core material in a helix configuration." (Accent added) (Kendall specification, column 1, lines 35-38.)

Here it will be understood by those skilled in the art that electroplated conductive material is a specific type of material. For example, Kendall in Column 8, lines 6-10, discloses an interconnect formed of a highly doped buried layer of semiconductor material. Further, studs 9, which form a substantial portion of Kendall's inductance, are either formed from the substrate (Figs. 2-6) or through selective crystal growth (Figs. 10-12). Clearly, the "electroplated conductive material" adds structural limitations that differentiate it from Kendall's conductive material. Electroplated conductive material, by definition, must be material that can be electroplated. Many different conductive materials cannot be electroplated. Thus, the term "electroplated conductive material" is a structural limitation. Even if, arguendo, Kendall's core 12 could be electroplated, the claim language "electroplated conductive material disposed within the trench to produce an inductance having sides and a bottom" would not be present.

The product-by-process cases cited by the Examiner, and indeed the entire product-by-process concept, applies to a claimed product, not to a component of the claimed product as is the situation in appellant's case. The cases cited by the Examiner state that "an old or obvious product produced by a new method is not patentable as a product". Appellant is not trying to patent electroplated conductive material, but is simply using the term "electroplated conductive material" to differentiate a portion of the invention from other conductive material that could be used.

The Examiner completes this portion of the ACTION by stating "no patentable weight will be given to those process steps which do not add structural limitations to the final product." While hundreds of examples of products defined by their unique processes could be cited (See appellant's Brief.), it is a well known fact that those skilled in the art (any art) accept the description of hard to describe items in terms of how they are produced. In some instances the description of an item is very difficult and it is necessary to describe the item in terms that include how the item was fabricated (see for example Ex parte Pantzer and Feier, 176 USPQ 141 (Bd. App. 1972)). Clearly, the term "electroplated conductive material" adds a structural limitation to the final product and should be given patentable weight.

#### SUMMARY

The subject application discloses and claims a new and improved integrated circuit that includes an inductance with a high quality (Q) factor. The inductance has a high Q factor because of the low permittivity structure that surrounds it. Nothing in any of the cited references suggests employing cavities adjacent the inductance to reduce the permittivity and improve the quality factor. Further, nothing in any of the cited references suggests the novel construction in which the inductance can be formed of electroplated conductive material. This feature greatly simplifies the fabrication and improves the operation.

Accordingly, it is respectfully asserted that appellant's claims 1-7, 28-33, and 37-51 are clearly allowable and the case is now in condition for allowance. Appellant therefore prays for the reversal of the final rejection and the allowance of the subject application.

Respectfully submitted,

Robert B. Davies

Robert A. Parsons

Attorney for Appellant

Registration No. 32,713

11 May 2004 340 East Palm Lane, Suite 260 Phoenix, Arizona 85004 (602) 252-7494